

Fig. 1B (Prior Art)

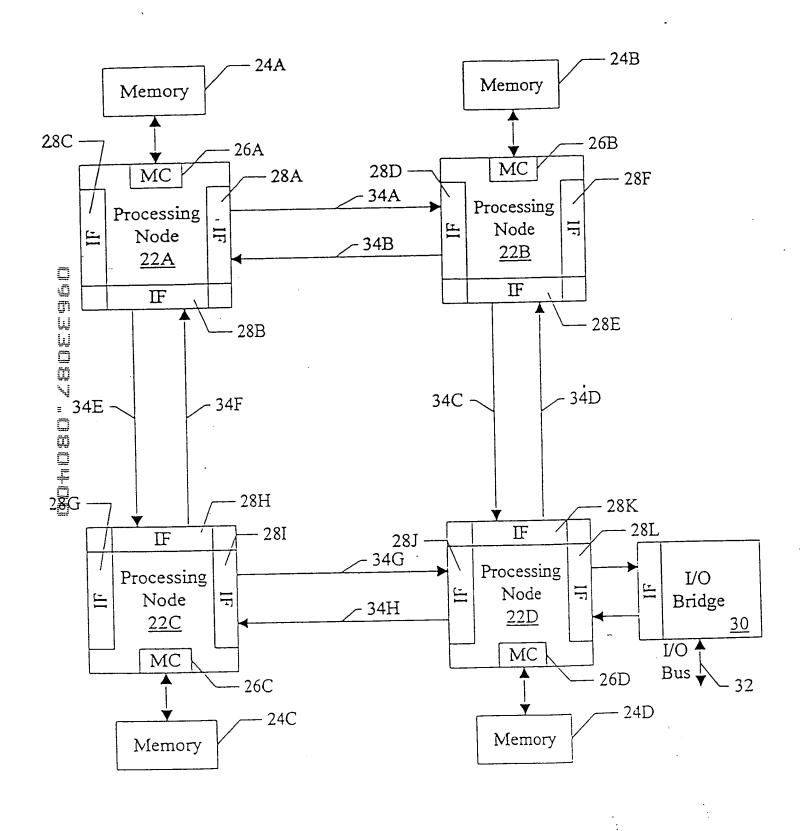


Fig. 2A

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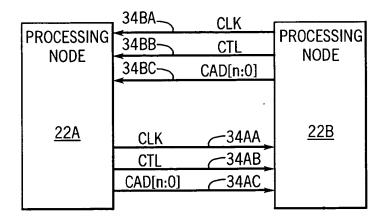


FIG. 2B

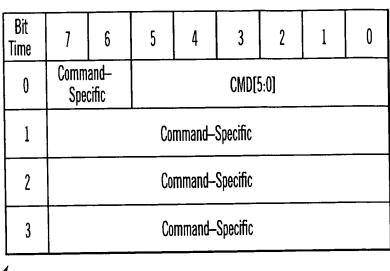


FIG. 3A

Bit Time	7	6	5	4	3	2	1 ·	0		
0	Src l [1:				CMD[	CMD[5:0]				
1	Command—Specific SrcNode[2:0]							]		
2		Command—Specific								
3	Addr[7:2]									
4		Addr[15:8]								
5		Addr[23:16]								
6		Addr[31:24]								
7		Addr[39:32]								

FIG. 3B

Bit Time	7	6	5	4	3	2	1	0	
0	Command- Specific			CMD[5:0]					
1	DestNode[2:0]			De Unit		Command- Specific			
2		Command-Specific							
3	Command-Specific								

FIG. 4A

Bit Time	7	6	5	4	3	2	·l	0			
0	Data[7:0]										
1	Data[15:8]										
2		Data[23:16]									
3	Data[31:24]										
4		Data[39:32]									
5,	:	Data[47:40]									
6		Data[55:48]									
7	Data[63:56]										

FIG. 4B

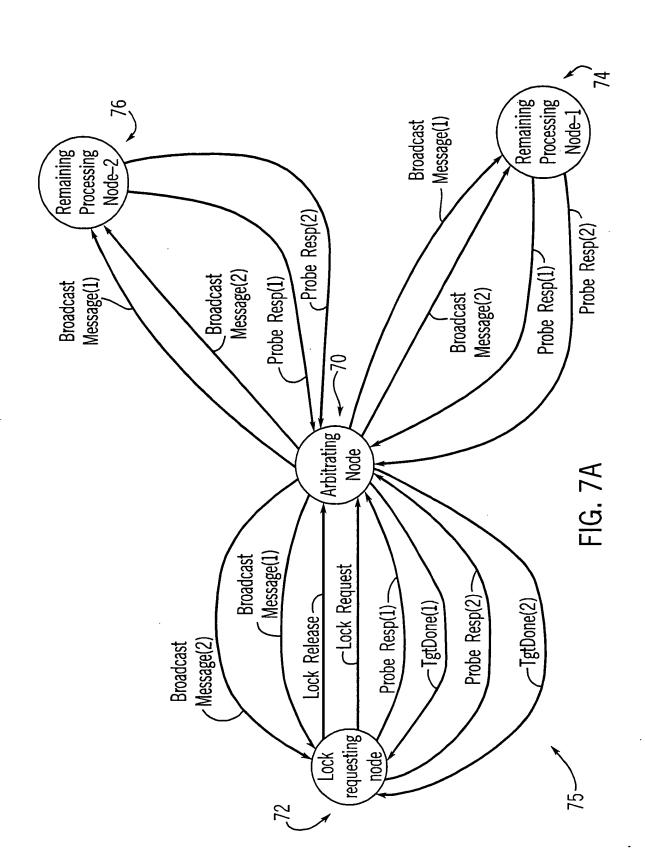
Bit Time	7	6	5	4	3	2	1	0			
0	-	Mask[7:0]									
1		Mask[15:8]									
2		Mask[23:16]									
3		Mask[31:24]									
4		Data[7:0] .									
5		Data[15:8]									
6		Data[23:16]									
7		Data[31:24]									
8+	Packe	Packet may contain up to eight double words of data									

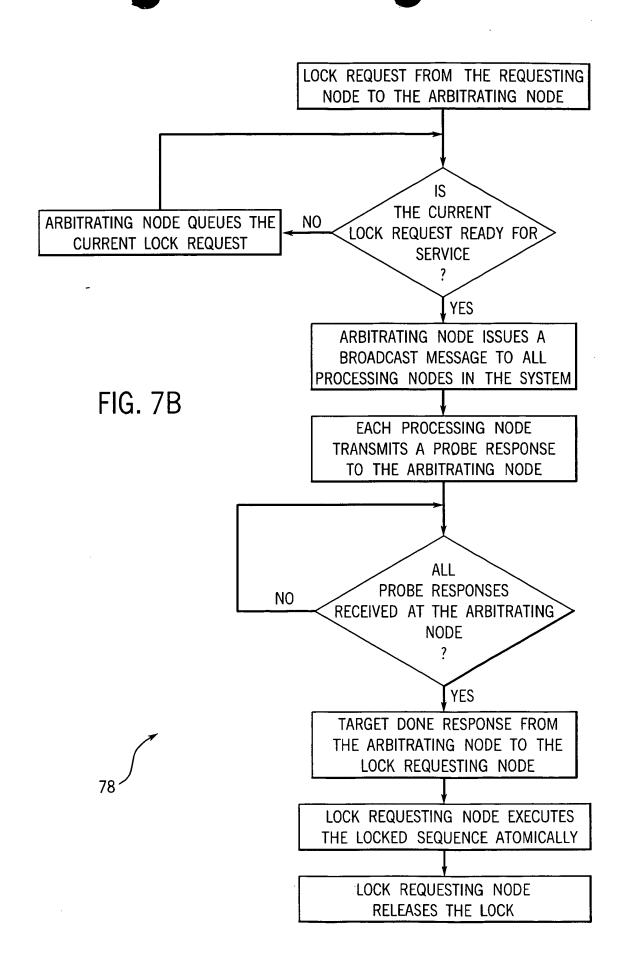
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FIG. 5

		<u> </u>
CMD Code	Command	Packet Type
000000	Nop	Info
000001	VicBlk	Request / Address / Data
000010	Reserved	_
000011	ValidateBlk	Request / Address
000100	RdBlk	Request / Address
000101	RdBlkS	Request / Address
000110	RdBlkMod	Request / Address
000111	ChangeToDirty	Request / Address
x01xxx	Write(Sized)	Request / Address / Data
01xxxx	Read(Sized)	Request / Address
100xxx	Reserved	_
110000	RdResponse	Response / Data
110001	ProbeResp	Response
110010	TgtStart	Response
110011	TgtDone	Response
110100	SrcDone	Response
110101	MemCancel	Response
11011x	Reserved	_
11100x	Probe	Request / Address
11101x	Broadcast	Request / Address
11110x	Reserved	_
111110	Reserved	_
111111	Sync	Info

FIG. 6

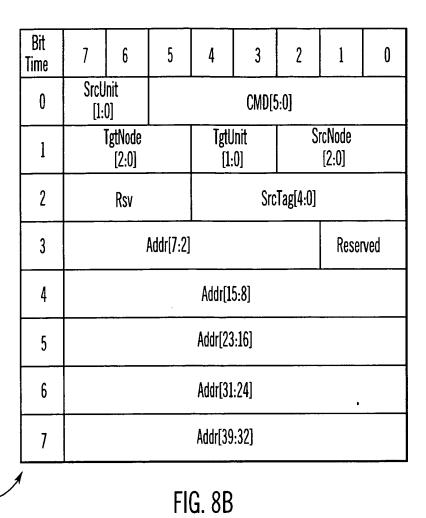




								i	
Bit Time	7	6	5	4	3	2	1	0	
0		Unit :0]			CMD	[5:0]			
1	DestNode [2:0]				DestUnit SrcNode [1:0] [2:0]			е	
2		Count :0]	Compat	SrcTag[4:0]					
3			Addr[7:	:2]		Lock	1	sk / t[3:2]	
4		Addr[15:8]							
5		Addr[23:16]							
6		Addr[31:24]							
7		Addr[39:32]							

FIG. 8A

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Bit Time	7	6	5	4	3	2	1	0	
0		SrcUnit [1:0]		CMD[5:0]					
1	DestNode[2:0]			DestU [1:0		SrcNode [2:0]			
2	Resen	Reserved Error			SrcTag[4:0]				
3	Shared	Reserved							

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Bit Time	7	6	5	4	3	2	1	0		
0	SrcUnit [1:0]			CMD[5:0]						
1	DestNode[2:0]			Dest [1:		SrcNode [2:0]				
2	Rese	rved	Error	SrcTag[4:0]						
3	Reserved									

FIG. 8D

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